CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. A SRAM cell comprising:

cross coupled pnp pull-up devices P1, P2, and npn pull-down devices N1, N2, with the P1, P2 devices being connected to a power supply VDD;

a first passgate coupled between a first bitline and the junction of devices P1 and N1, with its gate coupled to a wordline;

a second passgate coupled between a second bitline and the junction of devices P2 and N2, with its gate coupled to the wordline; and

wherein the N1, N2 devices are coupled through a P+ diffusion region to a ground.

2. The SRAM cell of claim 1, wherein the N1, N2 devices are coupled through a P+ diffusion region to ground at the intersection of the wordline and a P+ diffusion runner.

3. The SRAM cell of claim 1, fabricated on a chip entirely within a PC (polysilicon conductor) level, an M1 (first metal) level, and an M2 (second metal) level of a chip.

4. The SRAM cell of claim 3, fabricated with a straight PC level word line and a ground contact positioned at a peripheral boundary of the SRAM cell.

5. The SRAM cell of claim 3, fabricated with the M1 level containing global word lines and a power supply VDD, and the M2 level containing the bitlines and ground.

6. The SRAM cell of claim 1, fabricated with a P Well contact and an N Well contact.

7. The SRAM cell of claim 1, wherein the first and second passgates are npn devices.

8. The SRAM cell of claim 1, wherein a PC (polysilicon conductor) level wordline extends straight across a chip and crosses left and right legs of an M shaped RX (active silicon region isolated by trench isolation regions) region, with the crossing on the left defining the first passgate, with the wordline defining the gate and the RX region defining the source and drain regions of the first passgate, and with the crossing on the right defining the second passgate, with the wordline defining the gate and the RX region defining the source and drain regions of the second passgate.

9. The SRAM cell of claim 8, wherein left and right PC regions extend vertically on opposite left and right portions of the chip, a top horizontal portion of the M shaped RX region crosses the left PC region and defines the pulldown device N1, with the left PC region defining the gate and the RX region defining the drain and source regions of the pulldown device N1, the top horizontal portion of the M shaped RX region crosses the right PC region and defines the pulldown device N2, with the right PC region defining the gate and the RX region defining the source and drain regions of the pulldown device N2, with a common source region between the pulldown devices N1 and N2.

10. The SRAM cell of claim 9, wherein a horizontal base of a W shaped RX region crosses upper portions of the left and right PC regions, a bottom horizontal portion of the W shaped RX region crosses the left PC region and defines the pullup device P1, with the left PC region defining the gate and the RX region defining the drain and source regions of the pullup device P1, the bottom horizontal portion of the W shaped RX region crosses the right PC region and defines the pullup device P2, with the right PC region defining the gate and the RX region defining the source and drain regions of the pullup device P2, with a common source region between the pullup devices P1 and P2.

11. A method of fabricating a SRAM cell comprising:

cross coupling pnp pull-up devices P1, P2, and npn pull-down devices N1, N2, with the P1, P2 devices being connected to a power supply VDD;

coupling a first passgate between a first bitline and the junction of devices P1 and N1, and coupling its gate to a wordline;

coupling a second passgate between a second bitline and the junction of devices P2 and N2, and coupling its gate to the wordline; and

coupling the N1, N2 devices through a P+ diffusion region to a ground.

12. The method of claim 11, including coupling the N1, N2 devices through a P+ diffusion region to ground at the intersection of the wordline and a P+ diffusion runner.

13. The method of claim 11, including fabricating the SRAM cell on a chip entirely within a PC (polysilicon conductor) level, an M1 (first metal) level, and an M2 (second metal) level of a chip.

14. The method of claim 13, including fabricating the SRAM cell with a straight PC level word line and a ground contact positioned at a peripheral boundary of the SRAM cell.

15. The method of claim 13, including fabricating the SRAM cell with the M1 level containing global word lines and a power supply VDD, and the M2 level containing the bitlines and ground.

16. The method of claim 11, including fabricating the SRAM cell with a P Well contact and an N Well contact.

17. The method of claim 11, including fabricating the first and second passgates as npn devices.

18. The method of claim 11, including fabricating a PC (polysilicon conductor) level wordline extending straight across a chip and crossing left and right legs of an M shaped RX (active silicon region isolated by trench isolation regions) region, with the crossing on the left defining the first passgate, with the wordline defining the gate and the RX region defining the source

and drain regions of the first passgate, and with the crossing on the right defining the second passgate, with the wordline defining the gate and the RX region defining the source and drain regions of the second passgate.

19. The method of claim 18, including fabricating left and right PC regions extending vertically on opposite left and right portions of the chip, a top horizontal portion of the M shaped RX region crossing the left PC region and defining the pulldown device N1, with the left PC region defining the gate and the RX region defining the drain and source regions of the pulldown device N1, the top horizontal portion of the M shaped RX region crossing the right PC region and defining the pulldown device N2, with the right PC region defining the gate and the RX region defining the source and drain regions of the pulldown device N2, with a common source region between the pulldown devices N1 and N2.

20. The method of claim 19, including fabricating a horizontal base of a W shaped RX region crossing upper portions of the left and right PC regions, a bottom horizontal portion of the W shaped RX region crossing the left PC region and defining the pullup device P1, with the left PC region defining the gate and the RX region defining the drain and source regions of the pullup device P1, the bottom horizontal portion of the W shaped RX region crossing the right PC region and defining the pullup device P2, with the right PC region defining the gate and the RX region defining the source and drain regions of the pullup device P2, with a common source region between the pullup devices P1 and P2.

21. A SRAM cell comprising:

cross coupled pnp pull-up devices P1, P2, and npn pull-down devices N1, N2, with the N1, N2 devices being connected to a ground;

a first passgate coupled between a first bitline and the junction of devices P1 and N1, with its gate coupled to a wordline;

a second passgate coupled between a second bitline and the junction of devices P2 and N2, with its gate coupled to the wordline; and

wherein the P1, P2 devices are coupled through a N+ diffusion region to a power supply VDD.

22. The SRAM cell of claim 21, wherein the P1, P2 devices are coupled through a N+ diffusion region to the power supply VDD at the intersection of the wordline and a N+ diffusion runner.

23. The SRAM cell of claim 21, fabricated on a chip entirely within a PC (polysilicon conductor) level, an M1 (first metal) level, and an M2 (second metal) level of a chip.

24. The SRAM cell of claim 23, fabricated with a straight PC level word line and a ground contact positioned at a peripheral boundary of the SRAM cell.

25. The SRAM cell of claim 23, fabricated with the M1 level containing global word lines and a power supply VDD, and the M2 level containing the bitlines and ground.

26. The SRAM cell of claim 21, fabricated with a P Well contact and an N Well contact.

27. The SRAM cell of claim 21, wherein the first and second passgates are pnp devices.

28. The SRAM cell of claim 21, wherein a PC (polysilicon conductor) level wordline extends straight across a chip and crosses left and right legs of an M shaped RX (active silicon region isolated by trench isolation regions) region, with the crossing on the left defining the first passgate, with the wordline defining the gate and the RX region defining the source and drain regions of the first passgate, and with the crossing on the right defining the second passgate, with the wordline defining the gate and the RX region defining the source and drain regions of the second passgate.

29. The SRAM cell of claim 28, wherein left and right PC regions extend vertically on opposite left and right portions of the chip, a top horizontal portion of the M shaped RX region

crosses the left PC region and defines the pulldown device N1, with the left PC region defining the gate and the RX region defining the drain and source regions of the pulldown device N1, the top horizontal portion of the M shaped RX region crosses the right PC region and defines the pulldown device N2, with the right PC region defining the gate and the RX region defining the source and drain regions of the pulldown device N2, with a common source region between the pulldown devices N1 and N2.

30. The SRAM cell of claim 29, wherein a horizontal base of a W shaped RX region crosses upper portions of the left and right PC regions, a bottom horizontal portion of the W shaped RX region crosses the left PC region and defines the pullup device P1, with the left PC region defining the gate and the RX region defining the drain and source regions of the pullup device P1, the bottom horizontal portion of the W shaped RX region crosses the right PC region and defines the pullup device P2, with the right PC region defining the gate and the RX region defining the source and drain regions of the pullup device P2, with a common source region between the pullup devices P1 and P2.

31. A method of fabricating a SRAM cell comprising:

cross coupling pnp pull-up devices P1, P2, and npn pull-down devices N1, N2, with the P1, P2 devices being connected to the power supply VDD;

coupling a first passgate between a first bitline and the junction of devices P1 and N1, and coupling its gate to a wordline;

coupling a second passgate between a second bitline and the junction of devices P2 and N2, and coupling its gate to the wordline; and

coupling the P1, P2 devices through a N+ diffusion region to a power supply VDD.

32. The method of claim 31, including coupling the P1, P2 devices through a N+ diffusion region to the power supply VDD at the intersection of the wordline and a N+ diffusion runner.

33. The method of claim 31, including fabricating the SRAM cell on a chip entirely within a PC (polysilicon conductor) level, an M1 (first metal) level, and an M2 (second metal) level of a chip.

34. The method of claim 33, including fabricating the SRAM cell with a straight PC level word line and a ground contact positioned at a peripheral boundary of the SRAM cell.

35. The method of claim 33, including fabricating the SRAM cell with the M1 level containing global word lines and a power supply VDD, and the M2 level containing the bitlines and ground.

36. The method of claim 31, including fabricating the SRAM cell with a P Well contact and an N Well contact.

37. The method of claim 31, including fabricating the first and second passgates as npn devices.

38. The method of claim 31, including fabricating a PC (polysilicon conductor) level wordline extending straight across a chip and crossing left and right legs of an M shaped RX (active silicon region isolated by trench isolation regions) region, with the crossing on the left defining the first passgate, with the wordline defining the gate and the RX region defining the source and drain regions of the first passgate, and with the crossing on the right defining the second passgate, with the wordline defining the gate and the RX region defining the source and drain regions of the second passgate.

39. The method of claim 38, including fabricating left and right PC regions extending vertically on opposite left and right portions of the chip, a top horizontal portion of the M shaped RX region crossing the left PC region and defining the pulldown device N1, with the left PC region defining the gate and the RX region defining the drain and source regions of the pulldown device N1, the top horizontal portion of the M shaped RX region crossing the right

PC region and defining the pulldown device N2, with the right PC region defining the gate and the RX region defining the source and drain regions of the pulldown device N2, with a common source region between the pulldown devices N1 and N2.

40. The method of claim 39, including fabricating a horizontal base of a W shaped RX region crossing upper portions of the left and right PC regions, a bottom horizontal portion of the W shaped RX region crossing the left PC region and defining the pullup device P1, with the left PC region defining the gate and the RX region defining the drain and source regions of the pullup device P1, the bottom horizontal portion of the W shaped RX region crossing the right PC region and defining the pullup device P2, with the right PC region defining the gate and the RX region defining the source and drain regions of the pullup device P2, with a common source region between the pullup devices P1 and P2.